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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/875,364	06/05/2001	Jung-Bae Lee	9898-173	7447

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/875,364	LEE ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *17-21,25 and 27-29* is/are allowed.

6)☒ Claim(s) *1-5,13,23,24 and 26* is/are rejected.

7)☒ Claim(s) *6-12,14-16 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 22 is objected to because of the following informalities: in line 4, "a auxiliary" should be changed to -- an auxiliary --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 13, 23-24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hase et al. U.S. Patent 5,636,254.

Regarding claim 1, referring to figure 2, Hase et al. teaches an on-chip signal processing delay circuit applied to a window adjustment circuit of a data acquisition circuit of a disk device, the circuit including window adjustment 1, a read phase locked loop (PLL) and data latch 5. In column 5, lines 15-45, figure 4 further shows a detailed structure of the delay line 2 of the window adjustment circuit 1 shown in figure 2.

Referring to figure 4, the window adjustment 18 includes: a reference signal input 7 and delay PLL 3. The reference signal input 7 and delay PLL 3 is representative of a first signal transmission path;

A read data 6 read from the disk and fed to analog variable delay A20, which outputs a delay signal A;

A control signal path 12, being an output from delay PLL 3, having a delay associated with the delay signal A. The control signal 12 corresponds to the claimed first temporary signal.

Hase et al. does not expressly disclose a controlling unit as set forth in the application claim. However, Hase et al. further teaches in figure 7 an embodiment of delay PLL 3 shown in figure 4. Delay PLL 3 in figure 7 compares reference signal, corresponding to the first transmission path, with control signal 12, corresponding to the claimed first temporary signal, to generate an adjustment control 12. In view of that, because Delay PLL 3 in figure 7 compares reference signal, corresponding to the first transmission path, with control signal 12, corresponding to the claimed first temporary signal, one of person of ordinary skill in the art would have recognized the interchangeability of delay PLL 3, taught in Hase et al. invention, for the controlling unit claimed in the patent application.

Hase et al. does not expressly disclose a controllable delay unit as set forth in the claim. Nevertheless, Hase et al. further teaches that a read PLL 4 receiving output from the variable delay circuit B 21 generates a synchronous

clock 11, which is fed to the data latch 5 together with a delay signal A 9. The delay signal 9 is latched by the synchronous clock signal 11 to be outputted as synchronous read data 8. In view of that, one of person of ordinary skill in the art would have recognized the interchangeability of read PLL 4 and data latch 5, as taught by Hase et al., for the controllable delay unit claimed in the patent application.

Regarding claim 2, in column 2, lines 54-67, Hase et al. discloses that the variable delay circuit of the first delay means is supervised according to a stable external reference signal such that the amount of delay matched a delay time decided by the external reference. The variable delay circuit of the second delay means delaying a signal as an object of processing is supervised according to the delay amount control signal obtained from the first delay means. In view of the foregoing teachings, the control signal 12, corresponding to the claimed auxiliary transmission path, is closely a replica of the read data path.

Regarding claim 3, as recited in claim 2, referring to figure 4, the variable delay circuit of the first delay means is supervised according to a stable external reference signal such that the amount of delay matched a delay time decided by the external reference. The variable delay circuit of the second delay means delaying a signal as an object of processing is supervised according to the delay amount control signal obtained from the first delay means. Hence, the controllable delay signal 10 can be configured

such that the control signal 10 substantially equals to delay signal A plus any internal delay time.

Regarding claim 4, delay PLL 3 inherently includes a voltage-controlled delay, see figure 7.

Regarding claim 5, in column 7 line 55 via column 8 line 30, figure 11 shows another embodiment in which the signal processing is applied to a write compensation circuit of a data write circuit. According to the aforementioned embodiment, the selector 151 receives a plurality of delay branches and selects one of the delay branches, responsive to the delay signal B 159. In this embodiment, selector 151 and analog variable N-tap delay 150 constitutes the claimed controllable delay unit.

Regarding claim 13, figure 7 illustrates an embodiment of the delay PLL 3 wherein the control signal 10 (see figure 4) is generated as a result of the reference signal 7, corresponding to the claimed first output signal, and the control signal, corresponding to the claimed first temporary signal.

Regarding claim 23, claim 23 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 24, claim 24 is rejected on the same ground as for claims 2 and 3 because of similar scope.

Regarding claim 26, claim 26 is rejected on the same ground as for claim 2 because of similar scope.

Allowable Subject Matter

3. Claims 6-12, 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 17-21 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 17, claim 17 is allowed over prior art of record since the cited references, taken individually or in combination, do not disclose a data latch circuit as set forth in the application claim.

5. Claim 22 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 22, claim 22 is allowed over prior art of record since the cited references, taken individually or in combination, do not disclose a signal transmission method as set forth in the application claim.

6. Claim 25 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 25, claim 25 is allowed over prior art of record since the cited references, taken individually or in combination, do not disclose a signal transmission circuit as set forth in the application claim.

7. Claim 27 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 27, claim 27 is allowed over prior art of record since the cited references, taken individually or in combination, do not disclose a signal transmission circuit as set forth in the application claim.

8. Claim 28 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 28, claim 28 is allowed over prior art of record since the cited references, taken individually or in combination, do not disclose a signal transmission circuit as set forth in the application claim.

9. Claim 29 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 29, claim 29 is allowed over prior art of record since the cited

references, taken individually or in combination, do not disclose a signal transmission circuit as set forth in the application claim.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ishibashi et al. U.S. Patent 5,621,774 discloses "Method And Apparatus For Synchronizing Parallel Data Transfer".

Cao et al. U.S. Patent 6,240,139 discloses "Apparatus And Method For Repeating Simultaneously Transmitted Signals On A Single Transmission Path".

Tanji et al. U.S. Patent 6,307,906 B1 discloses "Clock And Data Recovery Scheme For Multi-channel Data Communications Receivers".

Eto et al. U.S. Patent 6,630,850 B2 discloses "Semiconductor Integrated Circuit Including Command Decoder For Receiving Control Signals".

Isobe et al. U.S. Patent 6,078,623 discloses "Data Transmission Apparatus And Method".

Klimek et al. U.S. Patent 5,724,392 discloses "Automatic Path Delay Compensation System".

Takahashi U.S. Patent 6,370,200 B1 discloses "Delay Adjusting Device And Method For Plural Transmission Lines".

Fuji et al. U.S. Patent 6,169,435 B1 discloses "Semiconductor Integrated Circuit Device With Built-In Timing Regulator For Output Signals".

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh cong Tran 04/29/2005

KCT

Examiner KHANH TRAN